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# Microfabricated V-Groove Power Inductors for High-Current Low-Voltage Fast-Transient DC-DC Converters

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***Abstract*** **Microfabricated thin-lm inductors for high-frequency DC-DC power conversion at high currents and low voltages with fast transient response have been fabricated and tested. Inductors with a Co-Zr-O thin-lm core and a copper conductor have been fabricated in a silicon substrate. Prototype inductors have been characterized and applied in a 3.3-V-to-1.1-V, 8-A, 5-MHz DC-DC converter and have been shown to exhibit ef ciency of up to 89% and power density up to 96 W/cm$^2$ of substrate area. The inductors discussed in this paper emerge as strong candidates for high-ef ciency, high-power-density DC-DC converters for advanced digital systems such as microprocessors wherein the fast transient response of the microfabricated inductors can result in signi cant reduction in the converter's output capacitance.**

## I. Introduction

Microfabricated thin-lm inductors offer the possibility of signi cant performance improvements over present-day power inductor technology. Some thin-lm magnetic materials exhibit a high saturation ux density that enables fabricating magnetic devices with higher power handling capability per unit area of the inductor, a high resistivity that reduces eddy-current losses and low hysteresis that enables low-loss reversal of magnetization. Such bene ts, when combined with the economic advantages of batch fabrication, make it attractive to develop high-performance power magnetic components in or on a silicon substrate.

The microfabricated power inductors discussed in this paper termed as V-groove inductors consist of a triangular wire surrounded by magnetic material, embedded in a silicon substrate as sketched in Fig. 4. The inductors exhibit inductance in the 1-to-10-nH range and are well-suited for DC-DC converters operating between 1 MHz and 150 MHz. Though inductance of such small values may be easy to achieve, these inductors have been designed for low loss even at high DC currents of 8 A with ripple currents that are comparable in magnitude. Many prototype microfabricated thin-lm power inductors have been reported in [3]-[17]. However, most are typically limited by low ef cienc y (often 60% or lower) and low power density (often under 1 W of output power per cm$^2$ of substrate area). The V-groove inductors have been shown to achieve high ef ciencies at much higher power densities.

Power delivery to digital systems such as microprocessors requires 100 A or more at about 1 V [18]. There is signi cant need for small inductors with high performance in order to reduce output capacitor requirements while maintaining the microprocessor supply voltage to be stable within about 50 mV tolerance [18] in present-day voltage regulator modules. Previously, the fabrication of V-groove inductors with current-handling capability of 2 A DC in [19] with inductor ef cienc y (55%) close to predicted inductor ef cienc y (60%) and power density of 28 W/cm$^2$ was demonstrated. In this paper, we present microfabricated V-groove inductors implemented in a 3.3-V-to-1.1-V, 8-A ($I_{out}$), 5-MHz DC-DC converter with an inductor ef cienc y as high as 89% and power density as high as 96 W/cm$^2$.

## II. Magnetic Materials

Granular composite soft magnetic materials (nanoparticles of magnetic material dispersed in a non-conducting ceramic matrix), can be used to control eddy currents, and unlike the use of laminations, granular materials curtail eddy currents regardless of ux direction. The work in [20]-[22], for example, has proven that high performance is possible in vacuum-deposited materials with nanoscale particles of Co or Fe. A rigorous analysis comparing materials in [23] indicates that Co-Zr-O lms (Co nano particles in a zirconium-oxide matrix) are well suited for microfabricated power inductors with high power density and high ef cienc y. Hence Co-Zr-O thin lms were chosen as the core for the V-groove inductors. The Co-Zr-O based lms were deposited using magnetron sputtering. Two targets, one cobalt and the other zirconium, were co-

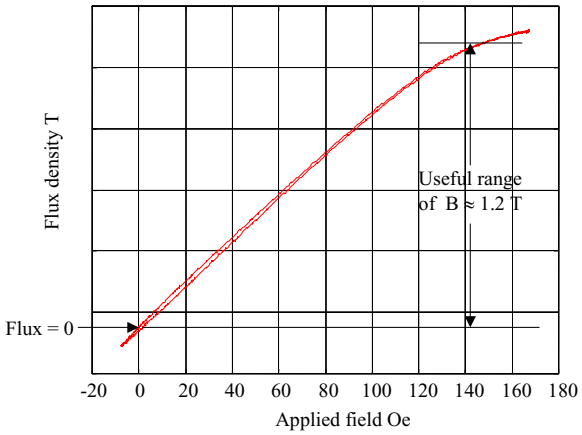


Fig. 1. $B$-$H$ characteristics along the hard axis of a 10-$\mu$m-thick sample of Co-Zr-O with unipolar excitation.

The $B$-$H$ characteristics along the hard axis of a 10-$\mu$m-thick Co-Zr-O thin lm were measured using a unipolar drive and are shown in Fig. 1. The material exhibits a high saturation ux density (1.3 T), very low coercivity (1 Oe) and a relative permeability of 80. The resistivity of the material was

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measured to be 600 $\mu\Omega$-cm using a four-point probe. This Co-Zr-O test-sample was deposited on a glass slide independent of the fabrication process which followed.

## III. Design of the V-Groove Inductor

The design process for the V-groove inductor is detailed in [23], [24], [25]; we provide a brief summary here. The dimensions of the inductor were calculated using material properties of the magnetic core viz., relative permeability ($\mu_r$), peak ux density ($B_{sat}$), coercivity (half-width of hysteresis loop), resistivity of the magnetic material and resistivity of the copper conductor. The thickness of the core was x ed at 10 $\mu$m by practical constraints. The design is saturation-limited; the perimeter of the cross-section of the V-trench (as shown in Fig. 9) is the magnetic path length and can be calculated from $B_{sat}$, $\mu_r$, number of turns, $I_{out}$ and the peak-to-peak amplitude of inductor ripple current ($\Delta i$) using Ampere's law. The width of the inductor can then be calculated from $\ell_{core}$ and the characteristic 54.7° orientation of the sidewalls of the V-grooves with respect to the horizontal. The choice of $\Delta i$ and the switching frequency ($f$) establishes the inductance requirement for the buck converter. A large $\Delta i$ and a large $f$ might seem to be rewarding choices for maximizing power density of the inductor but could lead to high losses in both the inductor and the MOSFETs. In [23], this tradeoff was explored and inductor and MOSFET designs with optimal $\Delta i$ and $f$ to maximize power density for a given ef cienc y were presented.

At 5 MHz, based on the analysis in [23], [24], [25], using the material properties of the test sample reported in Section II, and a conservative estimate of 2 $\mu\Omega$-cm for resistivity of copper, an optimized converter design with ef cienc y of 94% and a power density of 141 W/cm$^2$ was calculated for a 3.3-V-to-1.1-V, 8-A converter. The MOSFET design was based on a 0.13-$\mu$m, 3.3-V technology model derived from [26], [27] as discussed in [23]. The calculated converter design is presented in Table I.

TABLE I
CALCULATED AND TESTED DESIGNS OF V-GROOVE INDUCTORS.

| Description | Theoretical | Prototype |
|---|---|---|
| **CONVERTER PARAMETERS** | | |
| DC input voltage | 3.3 V | 3.3 V |
| DC output voltage | 1.1 V | 1.1 V |
| DC output current | 8 A | 7.87 A |
| Operating frequency | 5 MHz | 5 MHz |
| Duty cycle | 0.33 | 0.33 |
| **INDUCTOR PARAMETERS** | | |
| Number of turns | 1 | 1 |
| Thickness of magnetic material | 10 $\mu$m | 10 $\mu$m |
| Number of layers of magnetic material | 1 | 1 |
| **MATERIAL PARAMETERS** | | |
| Magnetic material | Co-Zr-O | Co-Zr-O |
| Conductor | Copper | Copper |
| Resistivity of magnetic material | 600 $\mu\Omega$-cm | |
| Resistivity of copper | 2 $\mu\Omega$-cm | |
| Relative permeability of core | 80 | 80(top)/50(sides) |
| Peak operating ux-density | 1.2 T | 1.2 T |
| Hard-axis coercivity (with unipolar drive) | 1 Oe | |
| **OPTIMIZED PARAMETERS** | | |
| Length of inductor | 11.4 mm | 16.4 mm |
| Length of magnetic path | 1.44 mm | 1.44 mm |
| Width of inductor | 0.55 mm | 0.55 mm |
| Inductance per 11.4 mm | 8 nH | 8.4 nH |
| Peak-to-peak amplitude of ripple current | 18.4 A | 11 A |
| DC winding loss | 160 mW | 184 mW |
| AC winding loss | 217 mW | |
| Eddy-current loss in core | 40 mW | |
| Hysteresis loss in core | 127 mW | |
| Total AC loss in inductor | 384 mW | 1.6 W |
| Total loss in high-side FET | 184 mW | |
| Total loss in low-side FET | 149 mW | |
| Total losses in FETs | 333 mW | 1.37 W |
| Ef cienc y of inductor | 94% | 83% |
| Power density of inductor | 141 W/cm$^2$ | 96 W/cm$^2$ |

## IV. Fabrication

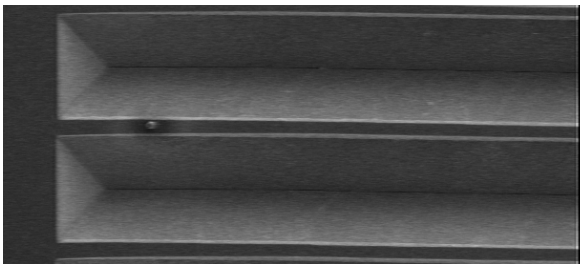
In this section the fabrication process for prototype V-groove inductors is described brie y; the process has been detailed in [28], [29]. We aimed to fabricate several 4.1-mm long inductors that were 550 $\mu$m wide and interconnect the required number of inductors in series to effect the required length of the optimized design listed in Table I (3 inductors for a total length of 11.4 mm).

V-shaped grooves were etched into a silicon substrate by an anisotropic etch as shown in Fig. 2. A 2-$\mu$m-thick insulating oxide layer was then grown on the substrate by thermal oxidation. Next, a 10-$\mu$m-thick layer of magnetic material (Co-Zr-O) was sputtered to form the bottom layer of the magnetic core as sketched in Fig. 3. A seed layer of chrome and gold was sputtered on the magnetic layer and patterned. The copper conductor was then electroplated with the help of the seed layer into the V-trench. The results of these steps are shown in Figs. 4 and 5. The surface of the wafer was non-planar at the end of the electroplating step. Chemical-mechanical polishing was used to planarize the surface of the wafer as shown in Figs. 6 and 9. Before deposition of another magnetic layer, photoresist was spun on the polished wafer and patterned to form bumps at the terminal ends of all the inductors as shown in Fig. 7. A 10-$\mu$m-thick layer of Co-Zr-O was then sputtered to complete the core around the copper to form a one-turn inductor as shown in Fig. 8. The photoresist bumps served as patterns for lifting off the nal layer of magnetic material to expose the underlying copper conductor at the terminal ends of each inductor to enable electrical contact through soldering. The terminals on the device were sized to be about 550 $\mu$m $\times$ 400 $\mu$m.

## V. Electrical Performance of the Inductor

The DC resistance of each 4.1-mm-long inductor was measured to be 0.74 m$\Omega$ using a four-terminal method; the predicted DC resistance was 0.90 m$\Omega$.

Individual inductors shown in Fig. 7 were soldered by a ip-chip process onto a custom-built ultra-low-impedance test x-ture [30] and small-signal measurements were performed using an impedance analyzer (Agilent 4294A). The inductors were deliberately chosen from different regions of the silicon wafer in order to investigate the uniformity of the fabrication process through electrical tests. The raw uncompensated inductance and AC resistance of several inductors were measured from 2 MHz to 14 MHz as shown in Fig. 10. An inductor with a measured inductance of 2.4 nH and with a measured AC resistance of 10.53 m$\Omega$ was chosen. After compensating for stray impedances, we determined that the inductance and AC resistance of the 4.1-mm-long, 550-$\mu$m-wide inductor were 2.61 nH and 7.55 m$\Omega$, respectively. The inductance and AC



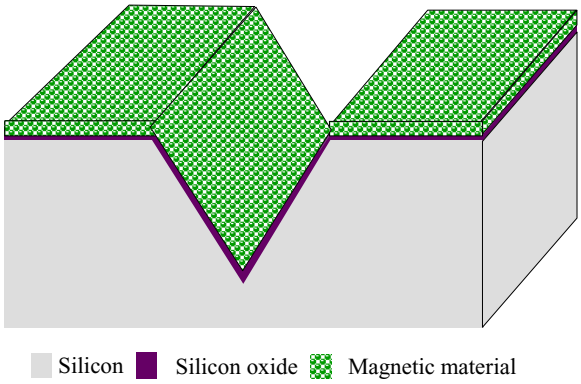



Fig. 3. Cross section showing the etched V-groove with an insulating oxide layer and a composite magnetic material on top of it.

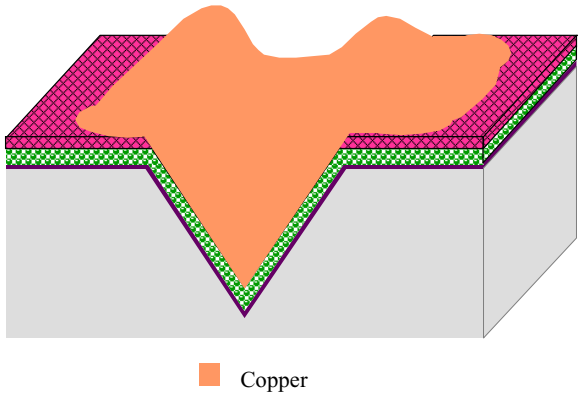



Fig. 4. Cross section showing a patterned seed layer and electroplated copper.

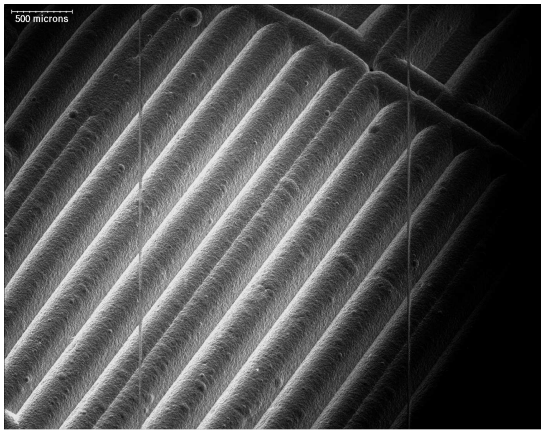



Fig. 5. Micrograph of substrate after electroplating copper in the V-grooves. Underlying substrate is not visible as sketched in Fig. 4.

resistance per 4.1 mm length of a 11.4 mm-long inductor in the calculated design listed in Table I were predicted to be 3.71 nH and 5 mΩ respectively. The chosen inductor exhibits 30% lower inductance per unit length and 50% higher AC resistance per unit length relative to the predicted values. The discrepancy between predicted and measured results is discussed later. At 5 MHz, inductance and resistance vary amongst the batch of tested inductors by 0.25 nH and 4 mΩ. Compared to the above-reported inductor, this is a variation of 10% in inductance and 40% in resistance and is attributed to non-uniformities in the fabrication process; variations in the repeatability of the soldering technique were determined to be 3 pH and 50 $\mu\Omega$ and are negligible compared to the measured impedances.

The in uence of DC bias superimposed on a ripple current in Co-Zr-O-based V-groove inductors was measured by repeating the small-signal measurements with a superimposed DC current. The high-frequency, small-signal inductance and AC resistance with DC bias were determined as shown in Fig. 11. Two inductors were tested. We observed that the a steady inductance was maintained up to at least 10 A DC. The inductance and AC resistance with and without DC bias are similar suggesting that drastic changes do not occur due to the effect of DC bias.

In summary, the 4.1-mm-long, 550-$\mu$m-wide microfabricated inductor exhibits 2.61 nH of inductance, 0.743 mΩ of DC resistance and 7.55 mΩ of AC resistance.

## VI. DC-DC Converter with Microfabricated Inductors

In [23], a buck converter design consisting of microfabricated inductors and MOSFETs (designed using a 0.13-$\mu$m process), was predicted to exhibit an ef cienc y of 91% and power density of 250 W/cm$^2$ operating at 16 MHz. The fabrication of MOSFETs in a 0.13-$\mu$m process was outside the scope of this project. Hence a prototype converter was realized using commercial MOSFETs. An IC consisting of high-side and low-side devices and gate drivers in a single package was used. A separate power supply for the gate-drive circuitry was used. Hence all measurements and predictions exclude gate-drive power. The MOSFET IC was optimized for operation much below 16 MHz; 5 MHz was chosen as the operating frequency for the converter. Even at 5 MHz, the dominant losses in the converter were expected to be in the MOSFETs and not the inductor. Our objective was to separate the MOSFET losses from the nal measurement on the converter by analytical and experimental procedures and demonstrate that the inductors have high performance.

The microfabricated inductors were assembled with a prototype 3.3-V-to-1.1-V, DC-DC converter which is shown in Fig. 12. The prototype board had four copper layers each 70 $\mu$m thick separated by 200 $\mu$m. The MOSFET IC and the

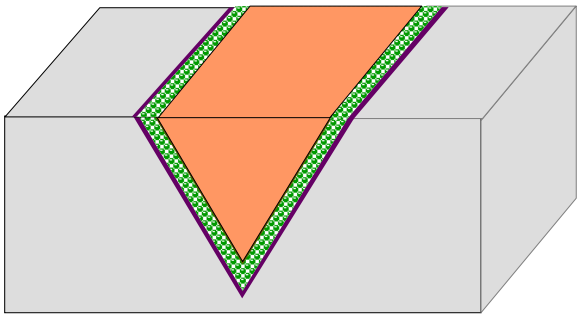


Fig. 6. A planarized wafer surface is achieved by chemical-mechanical polishing to remove excess copper from electroplating.

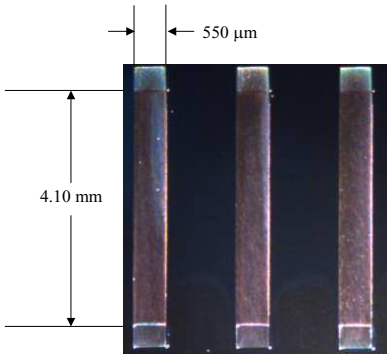



Fig. 7. Micrograph of top view of planarized microfabricated V-groove inductors prior to deposition of second layer of Co-Zr-O. Photoresist bumps can be seen at the terminal ends of each inductor.

silicon die containing the V-groove inductor were assembled on the board by ip-chip bonding. Multi-layer ceramic capacitors were soldered at the input and output terminals of the converter.

Fig. 13 shows a detailed circuit diagram of the prototype DC-DC converter; the impedance parameters for the various

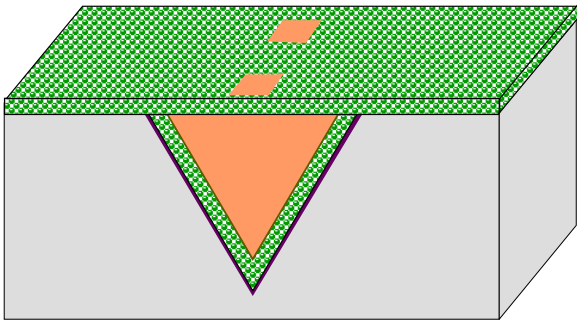


Fig. 8. More composite magnetic material is deposited to complete the V-groove inductor. Interconnection were accomplished with solder bumps through openings in the magnetic layer.

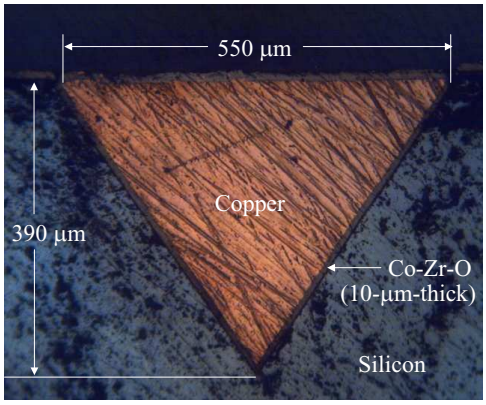



Fig. 9. Micrograph of cross-sectional view of V-groove inductor.

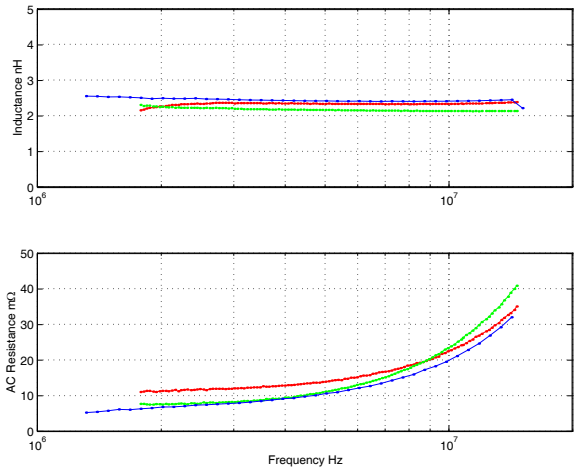



Fig. 10. Small-signal inductance and AC resistance characteristics of three different inductors. Results are uncompensated and include the impedance of the test xture.

DC current. The number of squares was calculated to be eight from the DC resistance measurement; the AC resistance of the output loop in the circuit was then calculated to be at least equal to 8 mΩ (corresponding to sixteen squares in the signal and ground traces). The calculation of the number of squares also allowed estimation of the parasitic inductance due to the board in the output loop in the circuit. Eight squares of copper interconnect with signal and ground layers separated by 200 $\mu$m, result in an inductance of approximately 2 nH. An analysis of experimental results discussed later indicate that the estimation of AC resistance and the inductance of the output loop in the board was reasonable. Also the output capacitors exhibit an equivalent series resistance (ESR) of 8 mΩ at 5 MHz; this is lumped with the 8-mΩ AC resistance of the output loop in the circuit. The ESR of the input capacitor was ignored relative to other impedances in the circuit. Input and output capacitor parameters were measured by small-signal analysis using the test xture discussed in [30].

Four inductors were connected in series to effect a total inductance of 10.4 nH, a total DC resistance of 2.97 mΩ and a total AC resistance of 30.1 mΩ in the output loop. The measured and predicted performance of the converter at 5 MHz are shown in Fig. 14. The peak ef cienc y of the converter was

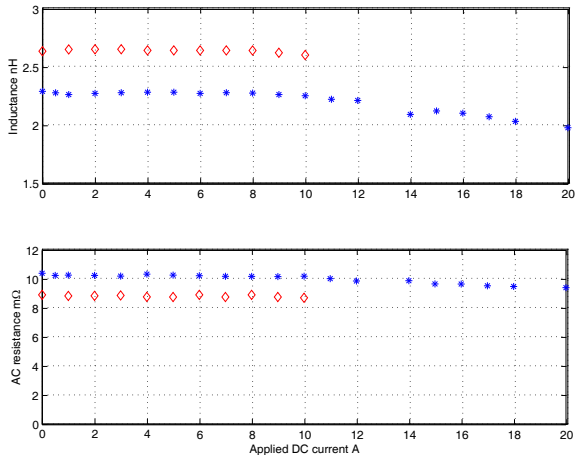



Fig. 11. Impedance characteristic of a microfabricated inductor measured at 5 MHz in the presence of an applied DC current.

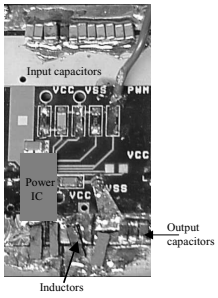



Fig. 12. Layout of converter.

observed to be about 78%. Using the values of impedances listed in Table II and the equations listed in the appendix, the performance of the inductor was determined by subtracting the theoretically calculated losses that are incurred in the rest of the circuit from the measured losses. This result is the measured performance of the inductor shown in Fig. 14. This is a conservative estimate of inductor performance in that it assigns any and all unaccounted for losses to the inductor.

Calculated and extracted results match well up to the peak efficiency in Fig. 14, but the measured inductor efficiency drops significantly above 5 A. This may be at least partially explained by losses in other parts of the circuit increasing

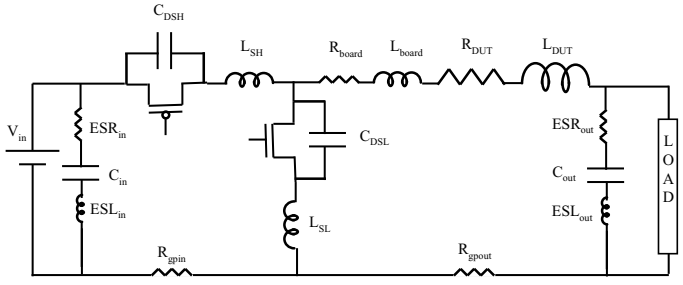



Fig. 13. Detailed circuit diagram of a DC-DC (buck) converter.

TABLE II
IMPEDANCES OF THE PROTOTYPE DC-DC CONVERTER. AC VALUES WERE MEASURED AT 5 MHZ.

| Parameter | Symbol | Value |
|---|---|---|
| DC resistance of inductors (4×0.743 mΩ) | $R_{DUTDC}$ | 2.97 mΩ |
| DC resistance of board | $R_{boardDC}$ | 2.16 mΩ |
| DC resistance of part of ground plane | $R_{gpin}$ | 0.58 mΩ |
| DC resistance of rest of ground plane | $R_{gpout}$ | 1.79 mΩ |
| AC resistance of inductors (4×7.55 mΩ) | $R_{DUTAC}$ | 30.1 mΩ |
| AC resistance of the board | $R_{boardAC}$ | 8 mΩ |
| On Resistance of high-side FET | $R_{DS-H}$ | 18.3 mΩ |
| On Resistance of low-side FET | $R_{DS-L}$ | 6.4 mΩ |
| Drain-source capacitance in MOSFET IC | $C_{DS-H}$+$C_{DS-L}$ | 3.5 nF |
| Inductance of high-side FET | $L_{HS}$ | 1 nH |
| Inductance of low-side FET | $L_{LS}$ | 1 nH |
| ESR of input capacitors | $ESR_{in}$ | 0.5 mΩ |
| ESR of output capacitors | $ESR_{out}$ | 8 mΩ |
| Inductance of inductors (4×2.61 nH) | $L_{DUT}$ | 11 nH |
| Inductance of output loop in board | $L_{board}$ | 2 nH |
| ESL of input capacitors | $ESL_{in}$ | 0.05 nH |
| ESL of output capacitors | $ESL_{out}$ | 0.35 nH |
| Input capacitance | $C_{in}$ | 20 $\mu$F |
| Output capacitance | $C_{out}$ | 25 $\mu$F |

in Fig. 11. Including ripple, the peak current in the inductor is expected to be above 10 A when the DC current is 5 A, so some decrease in inductance and corresponding increase in losses in the converter is expected above 5 A DC.

Fig. 15 shows theoretical predictions of losses in the circuit and inductor as a function of output power. The DC conduction loss in the inductors is the lowest of all the conduction losses. This demonstrates the superiority of microfabricated V-groove inductors in handling large DC currents with small power loss. At 5 W of output power, AC losses in the inductor (320 mW) and switches (720 mW) are very high. Reducing the AC resistance of the inductors and using optimized MOSFET designs are seen as key strategies towards improving the performance of the converter. The power density of the inductors range from 54 W/cm$^2$ (at peak inductor efficiency of 89%) to 96 W/cm$^2$ (at peak load with inductor efficiency of 83%). We report power density as the power handled per unit area occupied by the inductor excluding area of unused silicon. The prototypes as diced had an area of unused silicon that was comparable to the footprint area of the inductor. Hence, we also report a power density range of 27 W/cm$^2$ to 48 W/cm$^2$ when the area of unused silicon is included. With inductors spaced tightly as shown in Fig. 2, we expect power densities of 96 W/cm$^2$ and higher to be achievable in the future.

We estimated the inductance of the output loop to be close to 14 nH including the inductance of the inductors, the board, the equivalent series inductance of the output capacitor and the inductance of the lower switch ($L_{S1}$). The ripple current amplitude in the inductor was expected to be approximately 11 A. In order to confirm the prediction that the inductance of the output loop was 14 nH, the current in the inductors was measured. It was difficult to measure current without adding any stray inductance to the output loop. Hence, the current was measured by measuring the voltage drop across a sense resistor (0.56 Ω) placed in series with the inductors. The 0.56-Ω resistor was temporarily soldered in just for the ripple current measurement in place of an existing track in the board; hence no additional inductance was introduced by this approach. This measurement was performed independently of the efficiency

measurements reported in Fig. 14 since the power loss in this resistor was expected to be large. The resistance and inductive impedance in the output loop are comparable and result in an exponential variation of the inductor current. The inductor current was measured and the value of inductance required to effect the observed behavior (Fig. 16) in series with the 0.56-Ωresistor was determined analytically to be between 14 nH and 15 nH close to the predicted value.

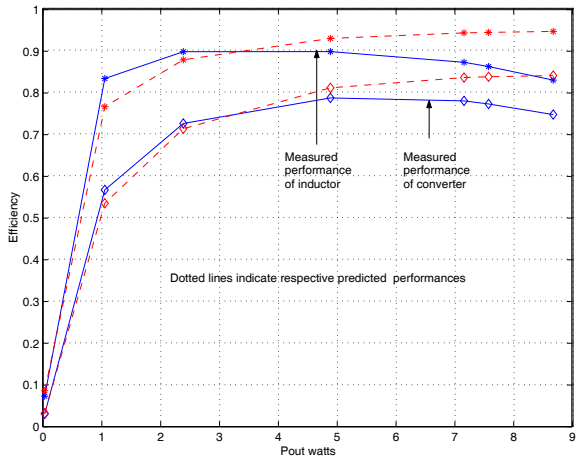



Fig. 14. Predicted and measured performance of the converter and inductors.

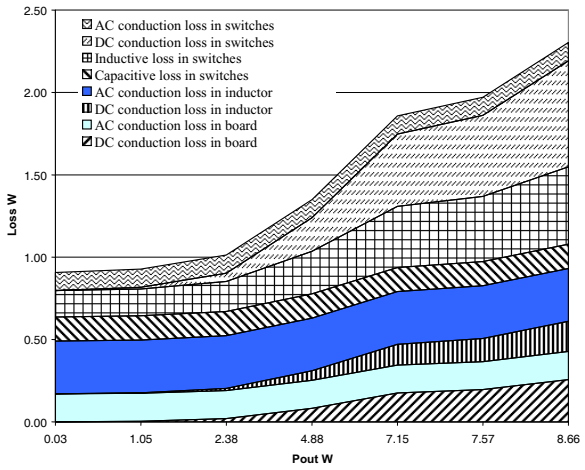



Fig. 15. Comprehensive theoretical breakdown of losses in converter.

In the small-signal measurements, we observed lower inductance per unit length of the prototype inductors than predicted. In order to investigate the discrepancy, a die containing Co-Zr-O only along the top of the V-groove was investigated separately and con rmed to exhibit ideal hard axis characteristics similar that shown in Fig. 1, with properties listed in Table I. Another die containing Co-Zr-O only along the sidewalls was tested separately. This die exhibited much higher coercivity and lower permeability than that of Fig. 1 suggesting larger losses than expected along the sidewalls of fabricated prototypes thereby leading to the larger measured AC resistance. To estimate the permeability of the Co-Zr-O along the sidewalls from the impedance measurements, we adjusted permeability in a nite-element analysis simulation

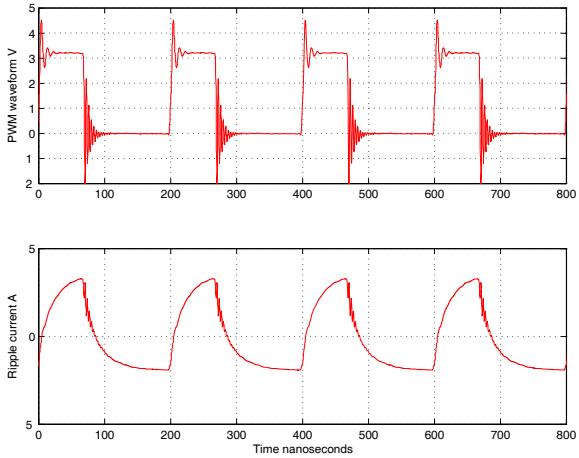



Fig. 16. Measured inductor ripple-current with large sense resistor in series with inductors. Corresponding PWM waveform is also shown.

to match the measured inductance. The relative permeability of the top magnetic layer was to set 80, and the permeability of the sidewalls was adjusted to match the measured 2.61 nH of a 4.1 mm long inductor. The relative permeability along the sidewalls was found to be nearly 50.

The low permeability of the sidewalls explains the fact that the measured inductance was lower than the original prediction. The low permeability and increased coercivity of the Co-Zr-O along the sidewalls are characteristic of stripe-domains [31]. In [32] sputter pressure and percentage of oxygen introduced in the system are cited as the main factors that affect the properties of Co-Zr-O thin lms. The work of nding the set of deposition parameters to yield stripe-domain-free material on slanting surfaces is an on-going research project.

## VII. Conclusion

Small-signal tests have been performed on prototype V-groove inductors. The prototypes were implemented in a 5-MHz DC-DC converter. Analyses of measured results indicate that the inductors in the converter achieve ef ciencies as high as 89% at a power density greater than 50 watts/cm$^2$ signi cantly better performance over most formerly reported microfabricated power inductors. Even with inductors exhibiting losses larger than expected, measured results on the DC-DC converter strongly indicate that V-groove inductors are attractive candidates for microprocessor power delivery. Work on improving the performance of the magnetic material on the sidewalls is an on-going project. As shown, parasitics in the DC-DC converter can seriously limit the performance of the converter. Methods to reduce these effects when combined with demonstrated performance of inductors can result in high performance converters with fast transient response an urgent need in eld of microprocessor power delivery.

## VIII. Acknowledgement

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## APPENDIX

At the switching frequency ($f$), the power loss in the drain-source capacitance was estimated as

$$P_{ds-capacitive} = 0.75(C_{DS1} + C_{DS2})V_{in}^2 f \quad (1)$$

Each MOSFET and the associated interconnects exhibits a parasitic inductance ($L_{S1}$ and $L_{S2}$). The inductive power loss at the switching frequency $f$ for each MOSFET was calculated as

$$P_{L_x-inductive} = \frac{1}{2}L_x(\mid I_{DC} - \frac{\Delta i}{2} \mid^2 + \mid I_{DC} + \frac{\Delta i}{2} \mid^2)f \quad (2)$$

where $L_x$ represents $L_{S1}$ and $L_{S2}$.

The AC conduction loss in the circuit shown in Fig. 13 was calculated as

$$P_{conduction-AC} = I_{rms-\Delta i}^2(R_{AC-H}D + R_{AC-L}(1-D)) \quad (3)$$

where $P_{conduction-AC}$ is the AC power loss, $R_{AC-H}$ is the AC resistance of the circuit when the high side-FET is on, $R_{AC-L}$ is the AC resistance of the circuit when the low-side FET is on and $I_{rms-\Delta i}$ is the RMS value of the triangular ripple current $\Delta i$.

The DC conduction loss in the circuit shown in Fig. 13 was calculated as

$$P_{conduction-DC} = I_{out}^2(R_{DC-H}D + R_{DC-L}(1-D)) \quad (4)$$

where $P_{conduction-DC}$ is the DC power loss, $R_{DC-H}$ is the DC resistance of the circuit when the high side-FET is on and $R_{DC-L}$ is the DC resistance of the circuit when the low-side FET is on.

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