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Found in *IEEE Conference on Global Sustainable Energy Infrastructure: Energy2030,* Nov. 2008, pp. .

IEEE Energy2030
Atlanta, Georgia, USA
17-18 November 2008

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***Index Terms*—electric vehicle, ultracapacitor, battery, hybrid, control**

***Abstract*—The energy storage system in electric vehicles (EV) must supply variable power levels and take regenerative power from braking. Ultracapacitors (UC) are more efficient than batteries for variable loads and recharging, but have a much lower energy density; the combination of these into a hybrid source can deliver better performance in an EV. We present several control systems, compare three active control schemes in-depth, and suggest a design. We describe a superior UC voltage control algorithm and a method of choosing optimal system parameters. Simulation validates the control approach of the complete system, and shows performance improvement of 48% by one metric. The test system includes a dc-to-dc converter with 97-98% typical efficiency.**

I. Introduction

Batteries often constitute the energy storage system in electric vehicles (EV), where they are subject to time-varying current demands, including acceleration and regenerative braking. Many efforts are being made to improve the performance of batteries for this application because the high cost, limited energy density, and short cycle lifetime of current battery technology hinders the viability of the EV. Batteries operate with greatest efficiency and have a longer lifetime when discharged at a low, steady rate. Although moving to a slower rate of discharge would improve the efficiency and lifetime of the battery, the average rate is set by the total energy needs and duration of a trip; reducing the energy demands of a given trip is beyond the scope of this paper, and increasing the duration of a trip (by driving slower) is generally undesireable. Given these constraints, reducing the variability of the current demands on the battery remains a viable approach to improve performance and cycle life. Several schemes to provide load-leveling for the batteries have been suggested, including flywheels, superconducting magnetic energy storage, and others [1]. One popular method is the addition of ultracapacitors (UC) as an auxiliary energy storage (AES) system to supply a portion of the power during high discharging or charging currents. Active control of the load fraction supplied from the AES provides superior performance over a passive parallel combination of the battery and UC [2]-[9]. Active control is usually accomplished with a dc-to-dc converter between the battery and the UC bank [6], [8], [10]-[14]. The goals of the control strategy are 1) to keep the UC voltage within a specified range and 2) to smooth the current in the battery for optimal battery performance and life.

This paper will: 1) present three control approaches to minimize load fluctuations on the battery and demonstrate that they are mathematically equivalent to each other; 2) present a method of UC voltage control and compare it to other voltage control schemes through simulation; 3) present a method for specifying the parameters for a control algorithm based on the specifications of the batteries and AES; 4) describe in detail the implementation of the control strategy derived in 1), 2), and 3) on an EV (electric vehicle).

II. Background

A variety of control strategies have been proposed, including simple rule-based algorithms [7],[10]-[12],[15], [16] linear filtering designs [9], [10], actively learning systems using in-car navigation systems to optimize behavior over frequented driving routes [17], and complex decision making schemes optimized with a neural network [11] or game theory [18]. Several other control strategies have been suggested for hybrid electric vehicles, some of which are only applicable to engine or fuel cell based designs [19]. Lu et. al. also suggest the direct connection of the UC to the load (and disconnection of the battery) during current peaks to avoid losses in the dc-to-dc converter and allow a smaller converter to suffice [20]. Optimization and active-learning-based control strategies usually include UC voltage limits and consider decreased AES system efficiency at lower voltages as an optimization factor in the system [11]. Linear filtering designs and rule-based control require a specified control algorithm for the UC voltage. Selecting an appropriate algorithm can improve the effectiveness of the AES system. Although a few UC voltage control designs are presented in the literature [9], [10], [12], [21], we are not aware of any study of the different possible strategies and how they affect system performance. UC voltage control strategies generally cause the state of charge (SoC) of the UC bank to tend towards some goal level. The goal voltage can be fixed or can vary; one scheme increases the goal SoC of the UC bank as the battery SoC and peak power ability decrease for constant combined peak power

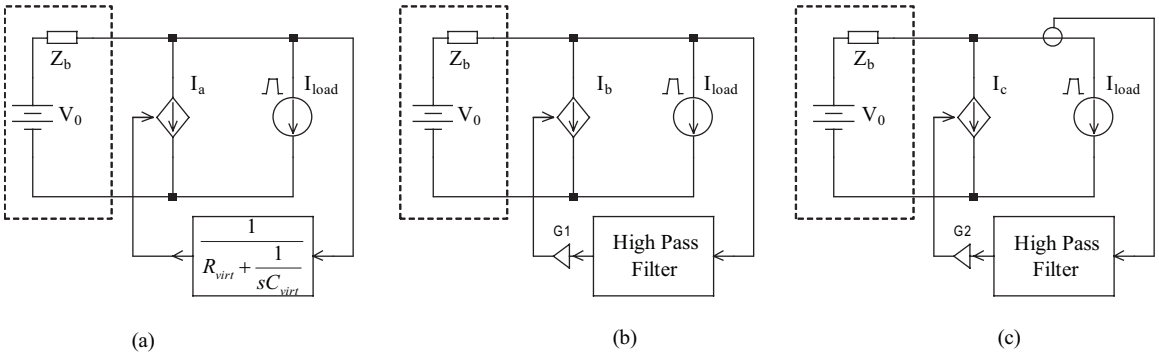

Fig. 1. Schematic representation of three possible control strategies. The dashed box encloses the battery. In each schematic, V_0, Z_b, and I_{load} are the battery open circuit voltage, battery impedance, and motor controller (load) of the drive system, respectively. The entire AES system, including the UC and dc-to-dc converter, is represented as a current source. I_a, I_b, and I_c are the current demands of the dc-to-dc converter; all other components comprise the control of the AES. In (a), C_{virt} is a very large capacitor with series resistance R_{virt} simulated by the UC bank and the dc-to-dc converter. In (b), voltage variations, amplified by the factor G_1, drive the current demand of the converter, stabilizing the voltage through negative feedback. In (c), the variable component of the input current to the motor controller, multiplied by a factor G_2, is the current command of the converter.

capability [12]; another monitors vehicle speed, keeping the capacitors at a higher SoC at low speeds to prepare for accelerations and a lower SoC at high speeds to allow room for energy from regenerative braking [10].

III. Battery/AES Load Division Control

Three simple strategies to smooth the battery load through control of the dc-to-dc converter current are: to monitor battery voltage and cause the AES system to simulate a huge capacitor C_{virt} with some series resistance R_{virt} connected across the battery (Fig. 1a); to use a voltage feedback system to suppress battery voltage variations (Fig. 1b); and to implement a feed-forward system that compares the instantaneous and average current demands of the motor controller and supplies the average demand from the battery, and the remainder from from the AES (Fig. 1c). These three strategies are mathematically equivalent if implemented with ideal components. Fig. 1 shows the terminals and the current on only the battery side of the dc-to-dc converter. None of these strategies address UC voltage management, which is discussed in Section IV.

The current commands given to the dc-to-dc converter (I_a, I_b, and I_c) of Fig. 1a, Fig. 1b, and Fig. 1c, respectively, are

$$I_a(s) = \frac{V(s)}{R_{virt} + \frac{1}{sC_{virt}}} = \frac{sC_{virt}R_{virt}}{1 + sC_{virt}R_{virt}} \cdot \frac{1}{R_{virt}} V(s) \tag{1}$$

$$I_b(s) = \frac{\tau_1 s}{1 + \tau_1 s} G_1 \cdot V(s) \tag{2}$$

$$I_c(s) = -\frac{\tau_2 s}{1 + \tau_2 s} G_2 \cdot I_{load}(s) \tag{3}$$

where $V(s)$ is the voltage across the load, $I_{load}(s)$ is the current demanded by the load, and τ_1 and τ_2 are the time constants of the first-order high pass filters in Fig. 1 (b) and (c) respectively. The current commands in (2) and (3) are multiplied by G_1 and G_2 respectively. We can see immediately that (1) and (2) are equivalent when:

$$G_1 = \frac{1}{R_{virt}}, \qquad \tau_1 = R_{virt}C_{virt} \tag{4}$$

It can also be shown that (2) and (3) are equivalent when, in terms of battery impedance Z_b,

$$G_2 = \frac{G_1 Z_b}{1 + G_1 Z_b}, \qquad \tau_2 = \tau_1(1 + G_1 Z_b) \tag{5}$$

Although these control strategies are mathematically equivalent with ideal elements, the feed-forward scheme (Fig. 1c) is inherently more stable than the other two approaches when delay in the response of the dc-to-dc converter and other elements are considered. We use the feed-forward control system (Fig. 1(c)) in our prototype. The selection of values for G_2 and τ is considered in Section V.

IV. Ultracapacitor Voltage Control

In most studies, UC voltage control is achieved by monitoring the voltage of the bank and adding a correction value to the current demand sent to the dc-to-dc converter, causing the voltage to tend towards a desired level [9], [10]. The voltage control must be capable of applying a strong enough current correction to ensure that the system cannot deviate beyond the voltage limits even under worst-case load conditions. For example, a system which applies a correction of ± 20 A to the demanded AES current could still be forced over the maximum UC voltage by sustained regenerative braking over 20 A. Since the additive term must be very large at the voltage extents to prevent deviations outside the limits, and since it is applied regardless of the AES current demanded, the UC voltage will bounce back from large deviations in UC voltage with high currents, causing large, unnecessary losses.

Our approach is to apply a multiplying factor (f) to current requests ($\tilde{I}$), rather than only an added term (Fig. 2). Two

different functions are applied to charge versus discharge requests; if the UC is near maximum voltage (V_{max}), only charging currents requests are attenuated while discharging current requests are allowed, and vice versa near the UC minimum voltage (V_{min}). This system ensures that the voltage cannot stray outside the set limits, since current requests pushing the voltage outside the limits will be multiplied by zero. We add a correction term (a in Fig. 2) to bring the UC bank to the nominal voltage (V_{mid}) during idle times. This term is weak since it is not responsible for preventing over or under voltage. The corrective factor we use is:

$$f(V_u, \tilde{I}) = \begin{cases} \left(\frac{V_{max}-V_u}{V_{max}-V_{mid}}\right)^n & for \quad \tilde{I} > 0 \ \& \ V_u > V_{mid} \\ \left(\frac{V_u-V_{min}}{V_{mid}-V_{min}}\right)^n & for \quad \tilde{I} < 0 \ \& \ V_u < V_{mid} \\ 1 & for \quad \tilde{I} < 0 \ \& \ V_u > V_{mid} \\ 1 & for \quad \tilde{I} > 0 \ \& \ V_u < V_{mid} \end{cases} \tag{6}$$

where n is a constant that defines the shape of the voltage control function; see Section V-B for a discussion of the effects of this parameter. The complete algorithm we apply is:

$$\hat{I}_c(\tilde{I}, V_u) = \tilde{I} \cdot f(V_u, \tilde{I}) + a \cdot (V_u - V_{mid}) \tag{7}$$

As treated in Section III, positive values of $\tilde{I}$ represent a request for current into the AES and negative values represent a discharging current. V_u is the present state of the UC voltage.

Fig. 3 shows the results of a simulation that demonstrates effective battery/AES load division and UC voltage control. The UC voltage does not stray outside the set limits. The action of the UC voltage control algorithm is most apparent during the large acceleration around $t = 200$ s, where the UC bank voltage approaches its minimum voltage limit. The battery is forced to take on additional load, characterized by the deviation of the battery current from the average current. Without the AES, the power factor[1] (PF) of the battery current is 0.54; the addition of the AES increases the PF to 0.80.

V. Optimization Considerations

The control constants of the system were optimized with numerical methods. A MATLAB simulation routine used input parameters, hardware specifications from the proposed test system, and a standard driving cycle (similar to Fig. 3) to calculate energy losses from the dc-to-dc converter, battery, and UC. Hardware specifications used for simulation are listed in Table I. The converter loss was modeled as constant gate drive power (whenever the converter is on) plus $(1 - \eta)$ multiplied by the power through the converter. The driving cycle was created from a simulation in Advisor Advanced Vehicle Simulator with a generic 1000 kg EV driven on the standard UDDS (Urban Dynamometer Driving Schedule). Data points were generated at 0.1 second intervals, and the MATLAB routine used linear interpolation on this data to produce a continuous load profile. Since the test system is an electric-assist bicycle (see Section VI for details), the motor power was scaled down by a factor of 20 to reduce the maximum power demand to about 1200 W; for comparison a typical power demand during maximum acceleration for the proposed test system was 900 W.

Numerical methods were used to optimize the input parameters of the simulation routine to produce the smallest loss. All control system paratemers were optimized, including the time constant (τ), n of (6), a of (7), V_{mid}, and others (discussed below).

[1]PF is the ratio of average power to the product of rms (root mean square) current and rms voltage: $PF = \frac{P_{avg}}{I_{rms} V_{rms}}$.

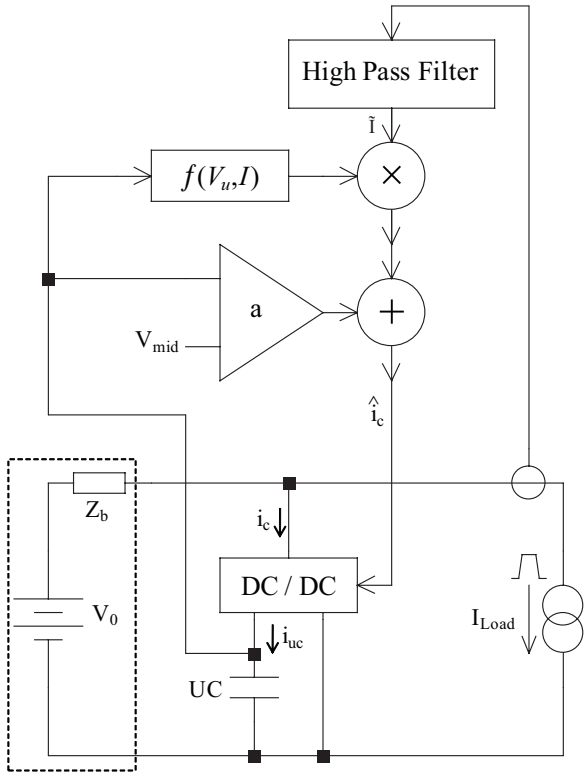

Fig. 2. Block diagram of the control system including UC voltage management.

TABLE I
HARDWARE SPECIFICATIONS USED FOR THE MODEL OF THE PROPOSED SYSTEM IN MATLAB SIMULATION.

Specification		Value	Description
V_{min}	=	30 V	Lower UC voltage limit
R_{UC}	=	0.053 Ω	UC bank ESR
I_{GD}	=	2.0 W	Gate drive power (avg.)
η	=	0.985	Converter efficiency (not incl. I_{GD})
V_{init}	=	45 V	Initial UC voltage
C	=	12.92 F	UC bank capacitance

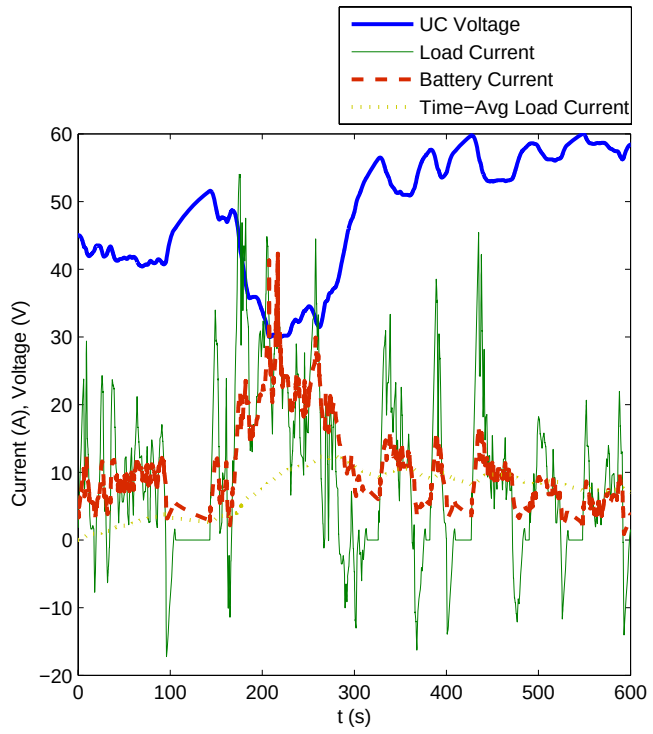

Fig. 3. First 600 seconds of a simulation of the full system demonstrating good voltage management. Load data is derived from the UDDS (Urban Dynamometer Driving Schedule). The system parameters are the optimal values for the simple battery model system, listed in the first column of Table III.

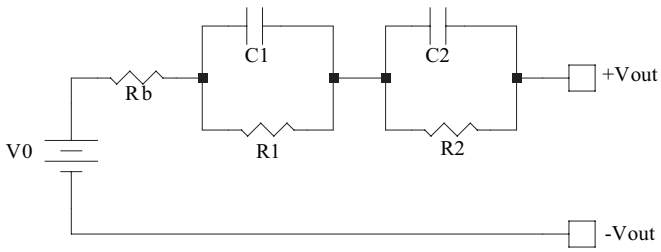

Fig. 4. Model for the complex behavior of the battery.

A. Frequency-Domain Analysis of Battery Losses

We model the battery as an ideal voltage source with a series resistance and a RC network to model transient response (see Fig. 4) [22]. Providing a thorough, defensible battery model is beyond our scope; our goal is to provide an estimation of the complex behavior of the test battery for the purposes of this discussion. We extracted the parameters from the test system's battery by discharging the battery at a constant 6 A for 15 minutes. Data was collected at 2 Hz. Prior to the test the battery was fully charged and then discharged at 6 A to 85% SoC. Only one test run was conducted, and only for the single steady discharge rate. The charging behavior of the battery was not tested; thus we assume it is a linear extrapolation of the discharging behavior. The model parameters were fit to the test data using a least-squares optimization in MATLAB. Table II lists the parameters extracted from the test system's battery.

TABLE II
PARAMETERS EXTRACTED FROM THE TEST SYSTEM'S BATTERY.

V_{b0}	=	26.028 V
R_b	=	0.1054 Ω
R_1	=	0.0879 Ω
C_1	=	12.293 F
R_2	=	0.1286 Ω
C_2	=	120.46 F

Fig. 5 plots resistive power loss in the test battery over a range of frequencies for a representative case based on the UDDS driving cycle. Power loss is calculated as: $P = I^2 Re(Z_b)$, where Z_b is the impedance of the battery. For comparison we plot a model with only the impedance of R_b (high-frequency ESR) of the battery included (ESR-only); this model neglects complex effects of the battery behavior (it does not include R_1, C_1, R_2, or C_2). At lower frequencies the complex effects of the complete battery model cause additional power loss over the ESR-only model. The plot is drawn on a logarithmic x scale; we multiply the dependent variable by frequency to keep the proportional relationship between area under the curve and power loss constant over the frequency range. Most of the energy loss occurs below 0.03 Hz and a significant portion of that loss is due to the transient behavior of the battery. We can see how much of the load variation is removed with a chosen time constant, and we can see what gains can be made by acheiving good efficiency with a longer time consant (which would generally require a larger UC bank). This can be tuned (and optimized for UC bank cost, weight, etc.) with numerical methods. We incorporate this transient battery behavior in the optimization model; the results are illustrated in Table III.

B. UC Voltage Control Parameters

Fig. 6 shows the effect of n on performance (simulated) of the AES with a step load of 20 A. With larger values of n the AES system begins to transfer load to the battery as soon as the UC deviates from the goal voltage, and gradually shifts the full load to the battery as the UC voltage reaches its limit. With smaller n, the AES takes close to the full load until the UC voltage deviates significantly from the nominal, at which point the load is transferred suddenly to the battery. The optimal value of n is dependent on the distribution of load pulse lengths; the ideal n will allow the AES to take the full load for short pulses, but not cause sudden spikes in battery current for longer pulses.

The strength of the additive term is controlled by a; it must be strong enough to prevent extended operation at inefficient UC voltage levels, but must remain weak to avoid unneeded energy transfer (and loss) between the battery and UC. Both

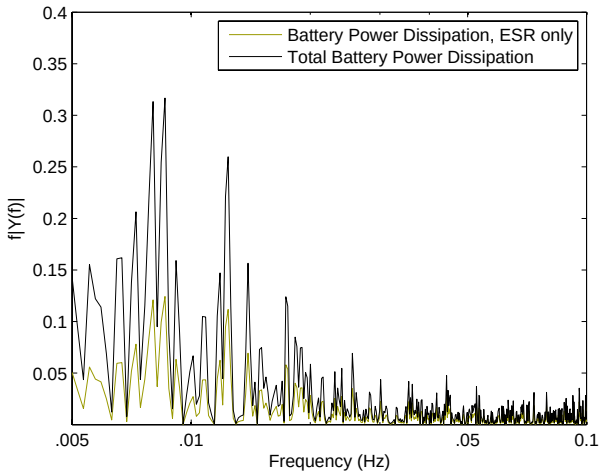

Fig. 5. Resistive power loss in the battery based on a Fourier transform of motor current demands during a simulation of the UDDS with a generic 1000 kg electric vehicle. For this illustration we use the model from [22] with parameters extracted from the test system's battery.

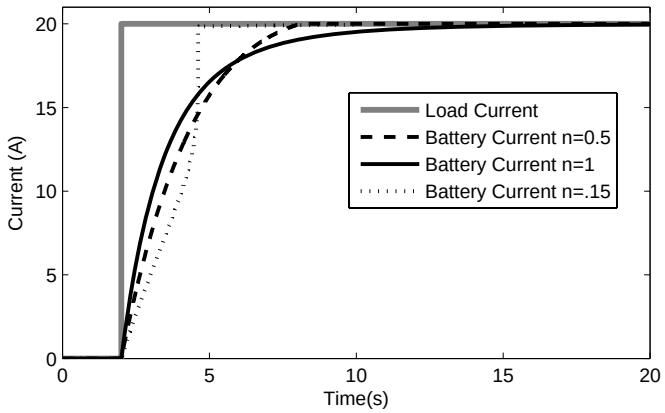

Fig. 6. Simulation of system behavior for $n = 1$, $n = .5$, and $n = .15$ with a 20 A step load. The time constant is set to infinity to eliminate the effects of time-averaging; the UC voltage control algorithm alone prevents the UC from taking the full load.

n and a are included in the numerical optimization.

C. Other Strategies to Maximize Efficiency

Since the dc-to-dc converter will draw power whenever it is running, it is advantageous to shut it off completely whenever the current demand of the converter is low. The actual shut-off current threshold (I_{SD}) is optimized as a control system parameter. Since we use a highly efficient converter, the optimal shut-off current is quite low, and the efficiency gain is small; with a less efficient dc-to-dc converter this feature will be more important.

It is more efficient to use both the battery and the AES to handle any spike in load, even if the AES could handle it alone. Since both the AES and the battery have resistance, the lowest losses will be achieved using both in parallel, with a certain portion of the load handled by each system. Thus the AES current demand is multiplied by a gain less than one, leaving the remaining portion for the battery. The value of the gain is also optimized numerically.

TABLE III
THE EFFECT OF A COMPLETE BATTERY MODEL ON LOSS AND OPTIMAL SYSTEM PARAMETERS.

Optimization battery model	Simplified	Complete
Loss predicted, simple bat. model (kJ)	12.8	12.8
Loss predicted, complete bat. model (kJ)	37.0	36.7
Power factor	0.79	0.80
Time constant (s)	752.8	993.6
n	0.043	0.055
a (A/V)	0.516	0.459
V_{mid} (V)	57.40	58.81
I_{SD} (A)	0.864	1.054
Gain	0.783	0.766

D. Optimization Results

Table III lists the optimal parameters for the simplified and the more complete battery models. The results from the optimization using the more complete battery model will probably yeild better system performance than those that use the simpler resistive model for the battery. The difference between these results demonstrates the importance of considering the complex behavior of the battery.

E. Comparison to Other UC Voltage Control Algorithms

Table IV compares the total system losses (simulated) for several different energy storage system configurations, including the proposed system, and a similar system presented in [10]. The simulation was again based on the UDDS. The total energy supplied by the energy storage system in each simulation was about 250 kJ. The physical components of the system presented in [10] are analagous to the proposed system, but the control algorithm differs in a few ways. The control in [10] modifies V_{mid} based on the vehicle speed, and uses only an additive term to control the UC voltage, while the AES current is a set fraction of the total demanded motor current plus or minus up to 20 A based on the UC voltage control term.

We adapted this control scheme to function in simulation for the purposes of comparison and attempted to optimize its performance for the simulation parameters; the algorithm for determining V_{mid} and the voltage control term were copied verbatim. The fraction of the total current demand supplied by the AES system was changed to its optimal value with the smaller system. Hard limits on the UC voltage were needed to prevent voltage deviations during the cycle; the additive term alone was not enough during large accelerations. While the performance of our adaptation of this control scheme was not as good as the proposed control strategy, it is very likely that a combination of the strategies could produce better results than either strategy alone.

TABLE IV
PERFORMANCE OF THE PROPOSED SYSTEM COMPARED WITH OTHERS VIA SIMULATION.

System	Simulated Loss (kJ)	(%)
Battery Only	55.3	22
Passive Hybrid	47.4	19
System Presented in [10]	40.3	16
Our System	36.7	14

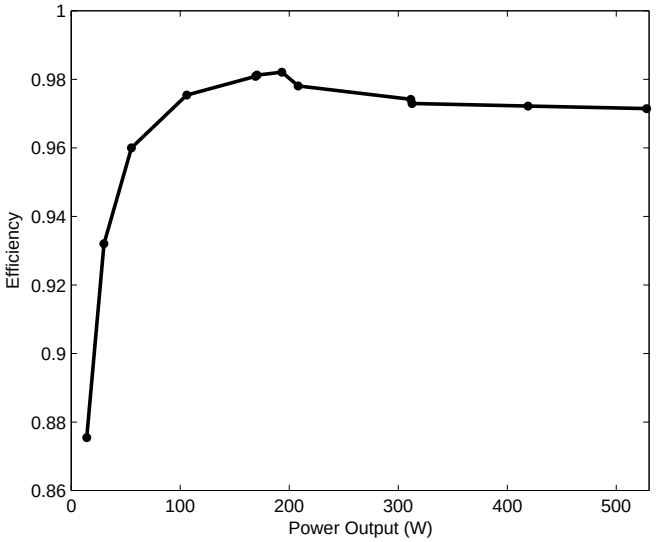

Fig. 7. Tested converter efficiency.

VI. IMPLEMENTATION

The system will be implemented on a bicycle fitted with a commercial electric assist system. The DC bus of the system is connected directly to a 24 V, 8 Ah nickel-metal hydride (NiMH) battery pack, with the AES system added in parallel with the battery as in Fig. 1c.

We have designed a bidirectional buck/boost dc-to-dc converter for 24 V at the main DC bus (we designate this as the output) and 30 V to 60 V on the UC bank (input). The design was optimized across factors including gate drive power, number of MOSFETS in parallel, frequency, inductor core and winding, and weight. Two low-ESR 160 μF, 75 V polyester film capacitors are used on the input. On the output are 27 multi-layer ceramic capacitors (20 μF each) connected in parallel. The optimized inductor uses an ETD59 core of 3C90 ferrite with five turns of 4200/44 (4200 strands of 0.0508 mm diameter) litz wire. Two parallel 75 V IRFB3077 MOSFETs are used for both the high-side and low-side switches. No heat sinks were needed in the design. The operating efficiency is about 98% depending on load (Fig. 7) and no-load power consumpsion is 2 W, which compares well to the predicted efficiency.

The control hardware for the system includes an analog PCB to provide current-mode control for the dc-to-dc converter and a digital controller that performs the higher-level system control. The analog board amplifies a current-sense signal from the converter and uses a current command signal and a PI controller to regulate the duty cycle of the converter. The analog PCB supplies gate drive to converter using two 2.5 A gate-drive optocouplers. The high-level controller monitors the load current and UC voltage, digitally filters the load current signal, implements the control equations (6) and (7), and provides the current command signal to the analog PCB.

The UC bank is made of four 15 V UC packs (Maxwell BPAK0052) in series, each of which contain six 2.5 V, 310 F cells in series. The UC bank is rated to 60 V, with 13 F of capacitance, and 53 mΩ total series resistance.

VII. CONCLUSION

An effective AES system on an electric vehicle must have a control strategy that directs load variations to the AES and limits the UC voltage, using proper system parameters for efficient functioning. Our load division control approach is equivalent to two other sensible approaches, and the proposed system for UC voltage limiting is effective, complete and incorporated into the overall control algorithm. Frequency-domain analysis of battery losses for the load profile can guide preliminary selection of system parameters to maximize the effectiveness of the AES system. Numerical optimization can be used to further refine the control system behavior. We have designed a control system for an AES system to provide load leveling for a primary energy storage system on electric vehicles, to be implemented and tested on an electric bicycle using a highly efficient dc-to-dc converter.

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