Fabrication of Thin Film V-Groove Inductors using Composite Magnetic Materials

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Abstract— **A new fabrication process is described for high-performance embedded or integrated inductors for power converters. The process includes etching V-grooves in a silicon substrate, depositing granular composite magnetic materials, electroplating and chemical mechanical polishing of copper conductors.**

I. Introduction

Inductors are essential components for efficient power conversion, but high-performance inductors are not available in conventional integrated circuit or packaging technologies. We have proposed designs for high-performance thin-film power inductors fabricated on a silicon substrate [1], [2]. These inductors could be embedded in thin-film packaging or integrated on the same die as silicon power devices, leading to a complete power converter in a single package in either case. In this paper we detail a complete fabrication process that was proposed in [3]. Although many prototype microfabricated thin-film magnetic components have been reported, [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20] most are limited by low efficiency (often 60% or lower) and low power density (often under 1 W of output power per cm^2 of substrate area). This is not adequate for the emerging challenges in microprocessor power delivery: high current requirements (up to 100 A or more) supplied efficiently at voltages near 1 V, with the requirement that the voltage must remain stable despite rapid changes in load current. The inductor is associated with fundamental performance constraints in a buck-converter for this application, and thus it is crucial to high-performance power delivery [1]. We have proposed microfabricated designs that can meet these requirements using new granular composite magnetic materials that reduce losses and a V-groove geometry to improve efficiency and power density [1], [2]. The designs are specifically optimized for performance in microprocessor power delivery, resulting in predicted power density of 158 W of output power per /cm^2 of substrate area and 95% efficiency for an 8 MHz, 3.6 V to 1.1 V converter.

II. Magnetic Materials

Microfabricated magnetic components are often made with thin layers of magnetic material to reduce eddy current losses. This is effective at controlling loss resulting from flux travelling in the plane of the film, but flux components out of the plane can still induce eddy currents that result in substantial losses [2], [21]. An alternative is to use fine particles of metallic magnetic material instead of multilayer thin films, similar in concept to conventional powdered iron materials. Although conventional powdered-metal materials have limited power performance at frequencies this high, recent work has shown that higher performance is possible in vacuum-deposited materials with nanoscale particles of Co or Fe [22], [23], [24], [25], [26]. These materials have usually been fabricated by reactive sputtering. A target such as Co-Zr is sputtered in an atmosphere containing a reactive gas such as O_2. Ideally, the Zr combines with the O and the Co forms a separate phase. The resulting material can have high performance at high frequencies, including relative permeability of 170 and Q of 60 at 100 MHz, with permeability maintained to about 1 GHz [25], attractive properties for both power and RF applications. In [19], an inductor application of these materials in an efficient high-frequency dc-dc converter was demonstrated at low power density. Such materials could be applied in improved designs to achieve much higher power density [1], [2].

III. Fabrication

In this section the fabrication process for this inductor is described. The proposed inductor designs are in the form of a triangular wire surrounded by magnetic material, embedded in a silicon substrate, as sketched in Fig. 6. The process is based on a V-trench formed by anisotropic etching of the silicon substrate. Composite magnetic material is deposited in the trench to form the core. Copper is filled in the groove to form the conductor and an overlayer of core material completes the inductor. The magnetic material is wrapped around a single wire and forms a one-turn inductor. Detailed design calculations for such inductors for microprocessor power delivery applications are discussed in [1]; inductors about 500 μm wide and 350 μm deep should be sufficient for such applications. Our intial fabrication tests are limited to smaller inductors 268 μm wide and 189 μm deep, in order to allow fabrication on standard-thickness three-inch silicon wafers.

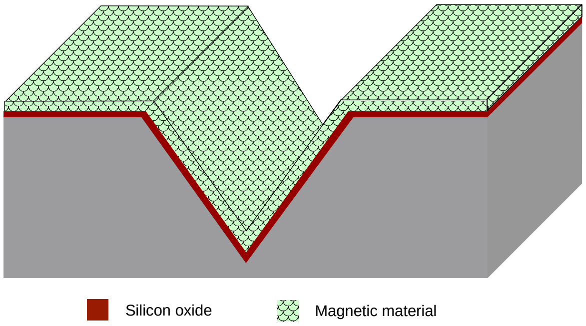

Fig. 1. Cross section showing the etched V-groove with two layers deposited on top of it: an insulating oxide layer followed by composite magnetic material.

The first step in the proposed fabrication process is to grow a masking layer to be used for the anisotropic etch of the V-groove. Thermally grown SiO_2 with an overlayer of chrome serve as a defect-free mask on Si surfaces. A combination of wet and dry oxidation is used to grow 2.5 μm of oxide and then approximately 500 Å of chrome is deposited by sputtering. The layers are then patterned using chrome etch followed by HF to form the mask for the anisotropic etch.

Anisotropic etchants of silicon include potassium hydroxide (KOH), tetramethyl ammonium hydroxide (TMAH), and ethylene diamine pyrocatechol (EDP). KOH is used as etchant for our process. The etch rates of various planes of silicon in an anisotropic etchant are found to decrease in the order $\{100\} > \{110\} > \{111\}$. The slowest etching planes are exposed as etching progresses [27], [28]. We used (100) wafers. If the mask opening is accurately aligned with the primary orientation flat, i.e., the [110] direction, after prolonged etching the $\{111\}$ family of planes is exposed down to their common intersection and the (110) plane disappears creating a V-groove with <111> oriented sidewalls at 54.74° to the (100) surface [28].

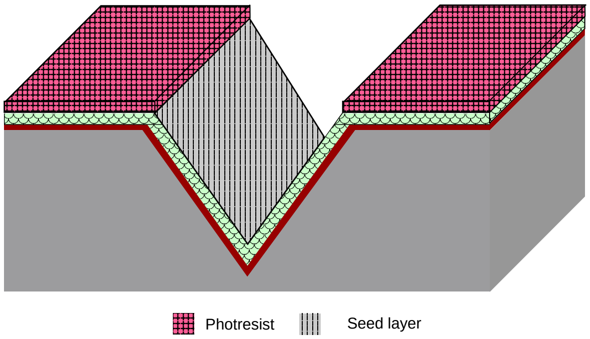

Fig. 2. A thin conductive metal seed layer that will be used for electroplating is deposited over the full wafer surface and then patterned with photoresist.

An overhang of oxide around the periphery of the V-grooves is observed at the end of the anisotropic etch step. This could pose problems for future steps of the fabrication process. The overhang is removed by etching all the remaining oxide on the wafer with HF. The next step is to grow another layer of silicon dioxide. The oxide layer will help in electrically isolating inductors from other devices on the same substrate. Composite magnetic material is deposited on this oxide layer by reactive sputtering. The thickness of the core was about 5 μm. The result of the first steps discussed above is shown in Fig. 1.

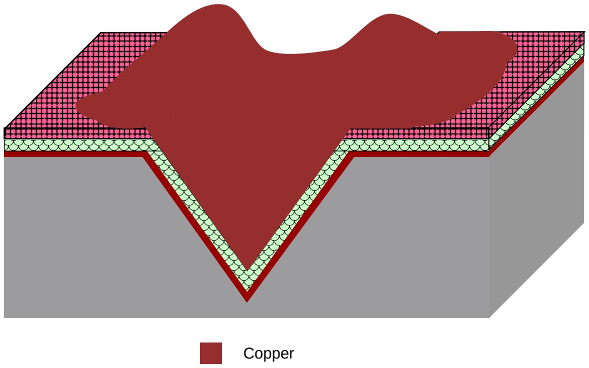

Fig. 3. Copper is electroplated into the V-grooves with the help of the seed layer.

Copper deposition is the next step in the fabrication. A thin seed layer of gold is deposited over the entire wafer surface following the deposition of the core. Photoresist is then spun on top of the wafer and developed to expose the V-grooves as sketched in Fig. 2. Copper is electroplated into the grooves with the help of the seed layer. The electroplating is stopped when the copper grows out and overfills the groove as shown in Fig. 3.

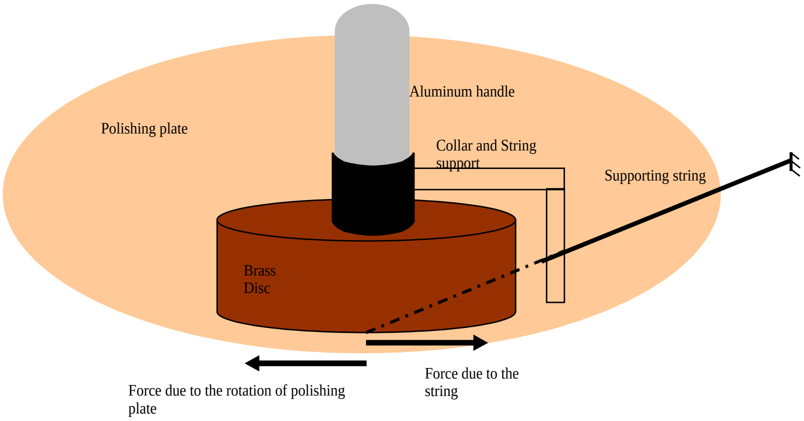

Fig. 4. Schematic of the in-house polishing setup for CMP of copper

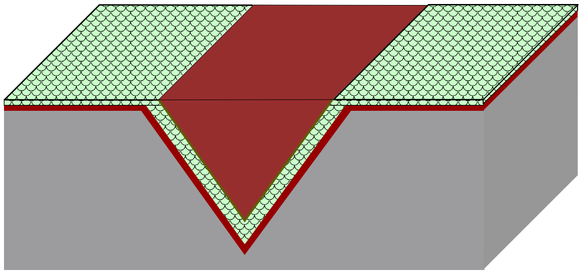

Fig. 5. A planarized wafer surface is achieved by chemical mechanical polishing to remove excess copper from electroplating.

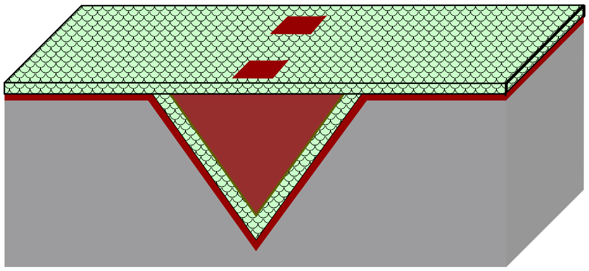

Fig. 6. More magnetic material is deposited to complete the V-groove inductor. Interconnection would be accomplished with another metal layer or solder bumps through openings in the magnetic layer.

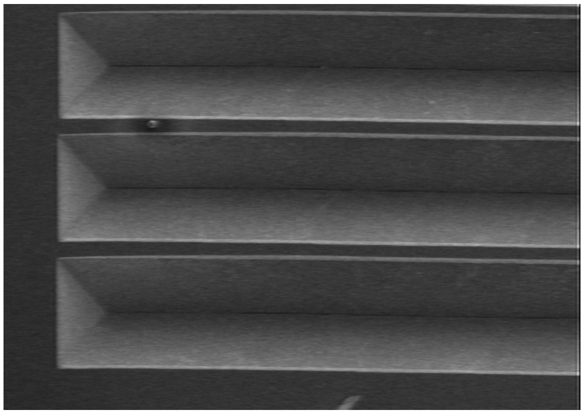

Fig. 7. SEM image of etched V-grooves in a silicon substrate

The copper is planarized by chemical mechanical polishing using an in-house polishing setup. The setup consists of a generic polisher and a weighted brass chuck 3” in diameter and 1.5” in thickness. The silicon wafer is attached to one side of the chuck by bonding wax. Uniform pressure is applied by adding weights to the top of the chuck. A polishing slurry consisting of ammonium hydroxide and alumina powder [29] is used with a hard polishing pad (IC 1000 from Rodel Inc.) stacked on a soft base pad (Subha IV from Rodel Inc.). The hard pad only polishes the highest structures on the wafer without conforming to the shape of the structures, thus ensuring planarity.

As the polisher rotates, a force acting on the chuck could produce a torque that would lead to uneven polishing. The chuck is held in place by a collar and string arrangement. The string is anchored at a height such that its force acts along a line through the center of the wafer as shown in Fig. 4. At this position we expect (theoretically) zero torque. This helps to achieve uniform polishing results. The wafer was also manually rotated at regular intervals to ensure uniform polishing along the radius of the pad. The polishing is continued until it exposes the core (Fig. 5). More magnetic material is then deposited as the next step to complete the core around the copper as shown in Fig. 6.

Contacts to the underlying copper can be made by removing the core material with a dicing saw. This contact area can be used for various interconnect strategies. For example, solder bumps could be grown, and the integrated or embedded power converters could then be connected to other chips using flip-chip technology. Fig. 7, Fig. 8 and Fig. 9 are images from a scanning electron microscope taken after etching V- grooves, electroplating and chemical mechanical polishing respectively. Results from tests conducted on the latest set of inductors at 8 MHz using low impedance test structures will be discussed in the final presentation.

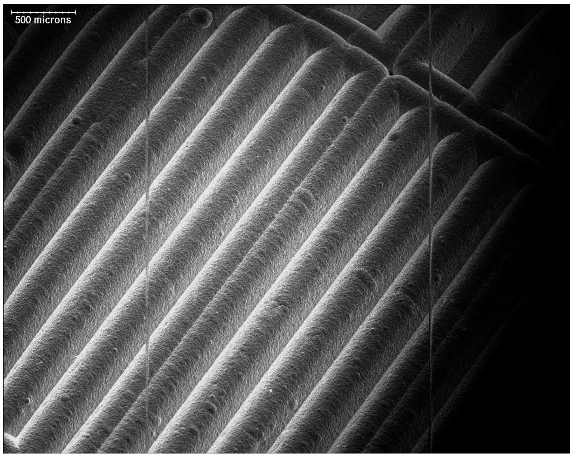

Fig. 8. SEM image of substrate after electroplating copper in the V-grooves

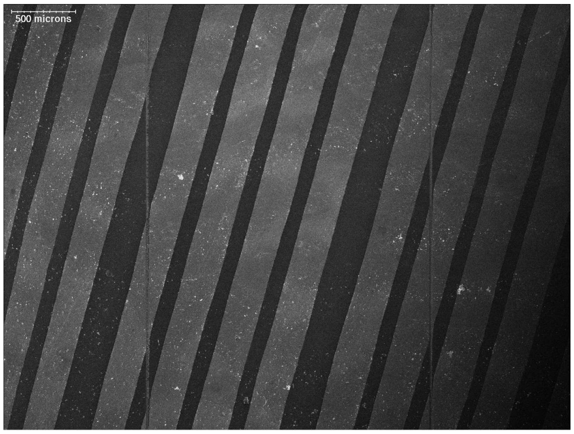

Fig. 9. SEM image of substrate after planarization of copper

IV. Conclusion

Inductor designs based on the V-trench process, using high-performance composite magnetic materials, are expected to enable compact low-profile microprocessor power converter circuits. A fabrication process leading to higher performance for embedded or integrated magnetic components in power applications has been described.

V. Acknowledgments

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