Converter and Inductor Design for Fast-Response Microprocessor Power Delivery

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Converter and Inductor Design for Fast-Response Microprocessor Power Delivery

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Abstract— **The fundamental constraints for fast-response buck converters for applications such as microprocessor power delivery are analyzed, with an emphasis on the role of the inductor. Optimum values of ripple ratio, and thus inductor value, are calculated. Based on this analysis, microfabricated inductor designs are analyzed, and an inductor design is proposed with predicted performance including power density of 158 W/cm^2 and 95% efficiency for an 8 MHz, 3.6 V to 1.1 V converter.**

I. Introduction

The high current requirements (up to 100 A or more) of future microprocessors pose a new challenge for power electronics design. This current must be supplied efficiently at voltages near 1 V, and the voltage must remain stable despite rapid changes in load current. Circuit and control innovations [1], [2], [3] have been developed to improve performance in this application. In this paper, we assume ideal control of a buck converter, and analyze the capability of the circuit to respond to a rapid load current step. We find that the inductor is associated with fundamental performance constraints, and thus is crucial to high-performance power delivery.

The second part of the paper then applies the analysis of converter performance to the design and evaluation of microfabricated thin-film inductors, as a technology that has the potential to provide the performance necessary for microprocessor power delivery [4], [5], [6], [7].

II. Ripple Ratio and Response to Load Steps

Consider a buck converter supplying a load with a large current step (either increasing or decreasing). We assume that advanced packaging and interconnect designs have minimized stray inductance such that one lumped capacitor represents bypass capacitance and converter output capacitance. Additional voltage disturbances could be added to those discussed here to account for packaging inductance. The magnitude of the ripple current in the inductor can be described by the ripple ratio (r_R);

$$r_R = \frac{I_{pp}}{I_{out}} \tag{1}$$

where I_{pp} is peak-to-peak ac ripple current, and I_{out} is the output current of the converter.

An increasing or decreasing load current step will result in an output voltage dip or rise, respectively. The direction of the load step affects the maximum possible output voltage change, except in the special case that the output voltage equals half the input voltage. With a converter output voltage less than half the input voltage, as would likely be the case for a converter supplying power to a low-voltage microprocessor, the worst-case output voltage deviation (ΔV) away from average output voltage is due to a load-current step from full load-current to zero load-current. Including both voltage disturbances due to steady-state ripple and due to the load current step, assuming worst-case timing of the load step relative to the converter switching, and assuming ideal control of the switches, we find the voltage excursion to be

$$\Delta V = \frac{I_{out}}{2Cf}\left(\frac{1}{8}r_R + \left(1 - \frac{V_{out}}{V_{in}}\right)\left(1 + \frac{1}{r_R}\right)\right) \tag{2}$$

where f is the operating frequency of the converter and C is the total bypass and output capacitance. The derivation of this expression is shown in the Appendix. With a high ripple ratio, the steady-state ripple voltage dominates, and the ripple should be reduced to reduce ΔV. However, lower ripple ratios (which correlate to a larger inductor) mean that the inductor current can only be changed slowly in response to a load step, and ripple should be increased to reduce ΔV. This trend can be seen in Fig. 1, where ΔV is plotted as a function of r_R for both positive-going and negative-going load steps. We see that there is an optimal ripple ratio which provides the smallest voltage deviation, which can be shown to be

$$r_R = 2\sqrt{2\left(1 - \frac{V_{out}}{V_{in}}\right)} \tag{3}$$

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A popular strategy to mitigate the effects of high ripple ratios on output ripple is to use multiple parallel buck converters with switch phases interleaved [2]. Using an analysis method similar to the one described above for a single buck converter, we have determined the voltage deviation for a multi-phase buck converter. Assumptions such as lumped inductances, capacitances, and ideal switching control were maintained; additionally each phase was assumed to have the same dc current and the same ripple ratio. Ideal switching during transients is assumed to turn on (or off) all phases in unison at the time of the load transient.

Unlike in a single-phase buck converter, the point of worst-case load transition does not necessarily occur at the switch transition in a multi-phase converter. During a load step the sum of the inductor currents slews at a faster rate than during normal output ripple, because of all the phases being turned on (or off) at once. For sufficiently high current slew rates, the difference in charge between load transients occurring at slightly different times is smaller than the amount of charge that flows in or out of the capacitor in the same period of time from normal output ripple. This is illustrated in Fig. 2. Areas A_1 and A_2 (corresponding to charge) are roughly equal, and thus both produce similar voltage deviations. However, before the load transition at time T_1 occurs, the area A_3 produces an additional voltage deviation, causing the maximum voltage deviation to occur if the load step happens closer to T_1 than to T_0. The time, ΔT, after T_0 at which a load step produces the worst-case voltage deviation for a decreasing load step is given by,

$$\Delta T = \frac{M_1(\Delta I + \frac{1}{2}I_{pp}) - M_2\frac{1}{2}I_{pp}}{M_1(M_2 - M_1)} \tag{4}$$

where ΔI is the output current load step, M_1 is the total inductor current ripple slope durring steady state, and M_2 is the increased slope generated by the ideal switching of all phases to respond to a load step. The correspoinding equation for and increasing load step is:

$$\Delta T = \frac{M_2\frac{1}{2}I_{pp} - M_1(\Delta I + \frac{1}{2}I_{pp})}{M_1(M_2 - M_1)}. \tag{5}$$

The voltage transient can be calculated from the areas of the triangles in Fig. 2. This can be combined with an expression for the initial voltage deviation at the worst-case load step time $T_0 + \Delta T$ to calculate total worst-case voltage disturbance, as shown for one example in Fig. 3.

From Fig. 3 we see that with a multiphase converter (four phases in this example), the minimum voltage disturbance occurs with very large ripple—in this case around a ripple ratio of 22. Thus the choice of ripple in a multiphase converter is, in practice, constrained by ripple-induced losses in the inductor and FETs rather than by considerations of voltage disturbance. The loss considerations in the inductor will be addressed in more detail in Section IV.

III. Converter Design for Fast Response

We now return to addressing a single-phase converter. The analysis in Section II addresses the optimum ripple ratio to maintain stable output voltage given output load

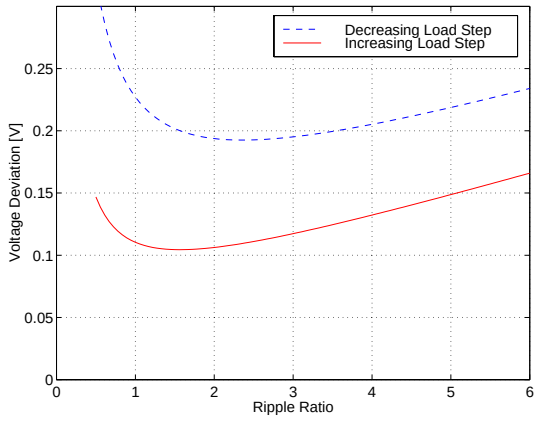

Fig. 1. Output voltage excursion in response to a load step from zero to full load current or from full load current to zero as a function of ripple ratio. Plotted for a single-phase buck converter with an input voltage of 3.6 V, an output voltage of 1.1 V, an output current of 30 A, a switching frequency of 8 MHz, and an output capacitance of 100 μF.

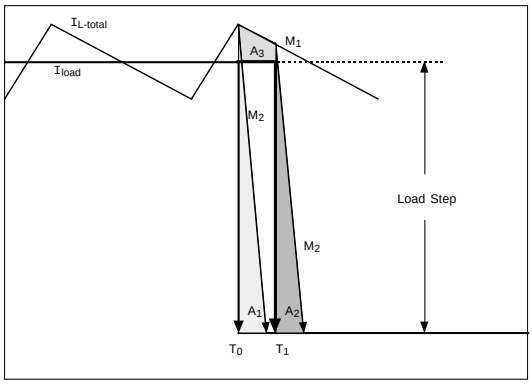

Fig. 2. Total inductor current and load current waveforms for a multiphase converter with a load current step, assuming ideal switching control. Shaded area A_1 represents excess charge transferred into the output capacitor if the load steps at time T_0. If the load steps at time T_1, the charge injected is area A_3 plus A_2. Thus, the worst-case timing for the step is no longer coincident with the peak current.

current steps. We now examine other converter parameters. If we select the optimum ripple ratio, and fix output current and input and output voltages, (2) shows that ΔV is proportional to $1/(Cf)$. With the optimum ripple ratio selected, the only remaining adjustment available to allow decreases in ΔV and/or C is to increase frequency. Thus, for high performance, we desire a circuit that operates at as high a frequency as practical, with a ripple ratio near the value specified by (3). As shown in Fig. 1, the optimum ripple ratio is typically around two. This high ripple ratio means that the inductor will have substantial ac current, and must have low ac losses in order to make the converter operate efficiently.

From the considerations above, it is desirable to use as high a converter switching frequency as possible. However, both power MOSFETs and inductors are generally considered to limit presently practical frequencies to about 1 MHz. Fortunately, progress on both fronts is likely to extend the practical frequency limit by perhaps an order of magnitude. For low-voltage converters, advanced CMOS technology intended for digital VLSI can be applied to improving power switches; indeed, experimental and commercial integrated power converters often use standard CMOS processes for power devices. Although reviewing the state of the art in this area is beyond the scope of this paper, it should be noted that silicon on insulator (SOI) is one promising technology that would enable fast-switching power devices with low gate charge and would allow much higher frequency converters.

The remaining critical issue, however, is the development of power inductors that meet the requirements of both low losses with high ripple current and operation at higher frequencies, in the 5-10 MHz range. The inductors should also be compact, reliable, and inexpensive. The remainder of this paper is devoted to developing inductor designs to meet these requirements.

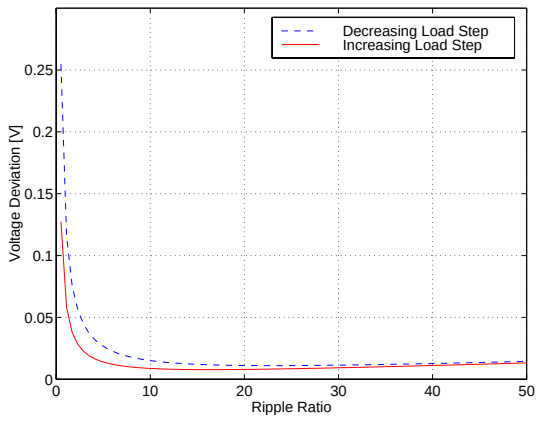

Fig. 3. Output voltage excursion in response to a load step from zero to full load current or from full load current to zero, plotted as a function of the ripple ratio. Plotted for a four-phase paralleled buck converter with an input voltage of 3.6 V, an output voltage of 1.1 V, an output current of 30 A, a switching frequency of 8 MHz per phase, and an output capacitance of 100 μF.

IV. Inductor Design

In [6], a microfabricated inductor was proposed for similar applications. The inductor would be fabricated using processing similar to semiconductor manufacturing. The design uses granular magnetic materials, a new type of soft magnetic materials, comprising nanoscale particle of magnetic metal in a ceramic matrix. These materials are characterized by high resistivities, high saturation flux densities, variable permeabilities, and low coercivities [8], [9], [10], [11], [12]. Here we analyze a design based on similar techniques and geometries, but based on the optimal ripple ratio for a single-phase converter chosen above, rather than the arbitrarily chosen ripple ratio used in [6]. We also present refined design calculations, including a Fourier representation of the current waveform, as used in [7], and consideration of more design variables.

For a given ripple ratio, the inductance required may be calculated as

$$L = \frac{\frac{V_{out}}{V_{in}}\left(V_{in} - V_{out}\right)}{r_R f I_2}, \tag{6}$$

or, for the optimal ripple ratio (3),

$$L = \frac{V_{out}\sqrt{2\left(1 - \frac{V_{out}}{V_{in}}\right)}}{4 f I_2}. \tag{7}$$

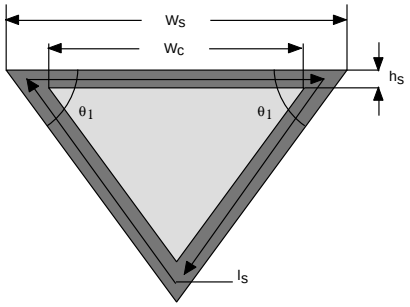

Fig. 4. Geometric parameters used in inductor calculations. h_s is the thickness of the magnetic material, W_s is the width of the magnetic magnetic material, W_c is the width of the copper conductor, ℓ_s is the core flux path length, and θ_1 is the angle created during an anisotropic etch (54.7°)

We now proceed to develop inductor designs based a design similar to that in [6], as shown in Fig. 4, to meet this inductance requirement. The design parameters for this "V-trench" inductor are length, width, core thickness,

and core properties. We fix a maximum practical thickness for the core material of 10 μm [7]. The maximum thickness for core material is a preferred choice for most designs of interest because, with high resistivity, eddy losses are not a major factor. This leaves three free variables: the width of the inductor, the length of the inductor, and the properties of the magnetic material. In particular, the permeability of the core material is of interest, and one of the advantages of granular magnetic materials is that their permeability can be varied through changes in material composition [13]. The three parameters (width W_s, length ℓ_L, and permeability μ_r) must be chosen in such a way as to satisfy two constraints: avoiding magnetic saturation and matching the inductance specification (6). This leaves one free parameter that may be varied to effect a desirable tradeoff between the primary performance parameters, which are efficiency and power density.

We choose to use the inductor width W_s as this free parameter. For a given choice of W_s, we then select the permeability of the core material and the width of the inductor based on satisfying the constraints of saturation and inductance, respectively [6]. Each choice of width then results in a complete design, and by calculating the performance of these designs, we can generate a curve of possible performance. An important part of the performance calculation is the prediction of losses, which are calculated as the sum of four quantities: core eddy current losses, core hysteresis, conductor dc losses and conductor ac losses. Our calculation of these quantities, detailed below, uses conservative material assumptions listed in Table I.

The core eddy-current loss and conductor ac loss calculation is similar to that described in [6], but improved by the use of Fourier analysis, as in [7]. The current waveform in the inductor is triangular and can be represented by a Fourier series. Each component's loss can be calculated and the results can be summed to increase the accuracy of the loss calculation. The hysteresis loss is considered insensitive to frequency, and so is excluded from the Fourier analysis. The Fourier expansion for the current amplitude of the k^{th} harmonic for the triangle waveform is

$$I_k = (\frac{\Delta I_{pp}}{2}) \frac{2sin(D\pi k)}{(\pi k)^2\ D(1-D)} \tag{8}$$

where

$$\Delta I_{pp} = r_R I_{out}. \tag{9}$$

Actual inductor current waveforms are not triangular but are slightly rounded due to power MOSFET turn-on and turn-off slewing. To account for this, the calculations used only the first five harmonics of the Fourier series to provide rounding of the waveforms [7].

Core eddy current losses are the sum of the losses due to the five Fourier ac flux components (B_{ac_k}),

$$P_{core-eddy} = \sum_k^5 \frac{w_k^2 B_{ac_k}^2 V_s h_s^2}{24 N_s^2 \rho_s} \tag{10}$$

where w_k is the frequency of the k^{th} harmonic in rad/s and V_s is the volume of the core. Eddy current losses may additionally be reduced by using multiple core layers, N_s. Granular magnetic materials have sufficiently high resistivity to make the use of multiple layers unnecessary. The core hysteresis loss is modeled as

$$P_{core-hysteresis} = \frac{3}{4} f V_s (4 B_{ac} H_c) \tag{11}$$

where H_c is the coercivity of the core and B_{ac} is the peak flux in the inductor. The factor of three-fourths is used to approximate the area of the actual hysteresis loop.

Winding losses in the copper of the inductor are modeled as dc and ac power dissipation. Dc power loss is simply calculated based on the cross sectional area of the copper, the length of the inductor, and the known dc current. Calculating the area of ac current flow in the conductor is more involved, because at high frequencies, skin effect cannot be neglected. We approximated the ac conduction region as roughly a skin depth around the perimeter of the copper, with correction factors as detailed in [6] and [14]. The ac resistance is calculated with this method for each of the five Fourier components, as discussed above, and the losses due to each are summed.

TABLE I

INDUCTOR DESIGN FOR 7 A, 1.1V OUTPUT CONVERTER.

Symbol		Value
W_c	Width of conductor	512 μm
h_s	Thickness of magnetic material	10 μm
ℓ	Length	8.8 mm
	Total device width	535 μm
A	Substrate area	0.049 cm^2
f	Operating frequency	8 MHz
B	Peak flux density	1 T
ρ_c	Conductor (Cu) resistivity	1.8 $\mu\Omega$-cm
ρ_s	Core (Co-Mg-F) resistivity	500 $\mu\Omega$-cm
μ	Core permeability	75 μ_0
P	Converter power output	7.7 W
r_R	Ripple Ratio	2.36
L	Inductance	5.8 nH
P/A	Power density	158 W/cm^2
R_{dc}	Dc resistance	1.71 mΩ
R_{ac}	Ac resistance	14.23 mΩ
Q	Quality factor	20
H_c	Coercivity	80 A/m
	Core loss	168 mW
	Conductor loss	239 mW
η	Efficiency	95%

Table I shows a set of specifications, and the results of our calculations based on these specifications. An impor-

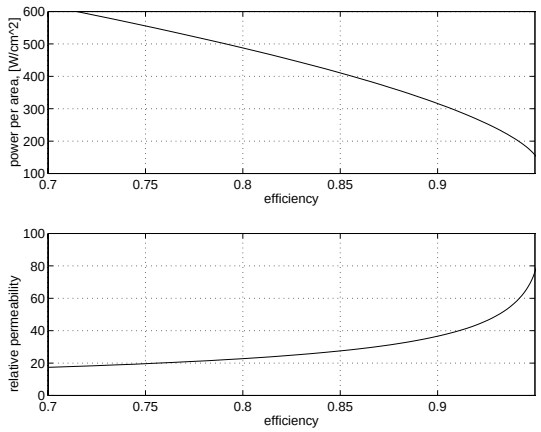

Fig. 5. Design tradeoff in V-groove inductor.

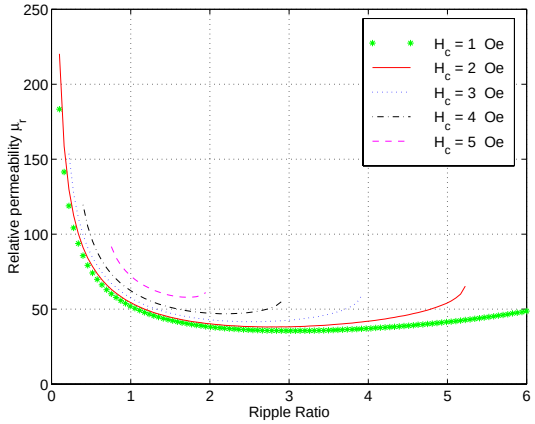

Fig. 7. Relative permeability of magnetic material needed the power density shown in Fig. 6.

tant design tradeoff, explored in Fig. 5, shows the maximum power density in watts per square centimeter of substrate area as a function of efficiency, and the required permeability of the magnetic material for optimum performance, also as a function of efficiency. The permeabilities, in the range of 20 to 100, are similar to the permeabilities found in nanoscale composite magnetic materials. The calculations have been extended to explore the

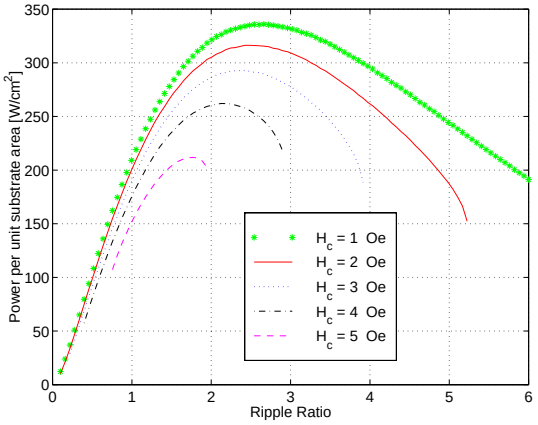

Fig. 6. Predicted inductor power per area as a function of coercivity and ripple ratio, based on a target efficiency of 90%. For some coercivities, 90% efficiency was not possible at all the ripple ratios shown, and so the curve does not span the entire range.

effect of various coercivities and ripple ratios on the efficiency and power per area of the inductor. Fig. 6 shows the power per area while Fig. 7 shows the require permeability for designs with various coercivities and ripple ratios. Satisfactory performance is possible with coercivities as high as 5 Oe. The optimal ripple ratio for high power density varies as a function of coercivity, but is similar to the optimal ripple ratio for minimizing output capacitance and output voltage disturbance for a single-phase converter, calculated in Section II.

V. Conclusion

The relationship between ripple ratio and total voltage disturbance given a load-current step has been explored, based on ideal control. Optimal ripple ratios to minimize voltage excursion for a single-phase converter have been found, and are typically around a peak-to-peak ripple of twice the dc output current. For multi-phase converters, optimal ripple ratios based on this criterion are much higher, and a lower ripple ratio will typically be chosen based on loss considerations. The performance we have calculated, assuming ideal control, will not be realizable with real control systems. However, it provides a useful benchmark for assessing performance of controllers.

Our calculations for an optimized inductor predict substantial performance improvements for microprocessor power delivery with power handling per substrate area of 158 W/cm^2 at 95% efficiency. Operating the converter at an optimal ripple ratio provides for the minimum necessary output capacitance to satisfy an output voltage regulation specification in a single-phase converter. These advances will allow high performance power delivery for future microprocessors.

Appendix

The expression for the maximum voltage deviation is derived as follows. First, we consider a decreasing load-current step of magnitude ΔI, occurring at the time of peak inductor current in the normal ripple cycle. Starting from the time of the preceding ripple current zero crossing (inductor current equal to load current), we can integrate the charge flowing into the capacitor. First, as the inductor current increases to its peak, we get a charge contribution

of

$$Q_1 = \frac{1}{2}\left(\frac{I_{out} r_R}{2}\right)\left(\frac{\frac{V_{out}}{V_{in}}}{2f}\right) \quad (12)$$

The additional charge added while the inductor current slews down by $(\Delta I + \frac{I_{out} r_R}{2})$ to match the new load current is

$$Q_2 = \frac{1}{2}\left(\frac{L}{V_{out}}(\Delta I + \frac{I_{out} r_R}{2})\right)(\Delta I + \frac{I_{out} r_R}{2}). \quad (13)$$

We can substitute for L using

$$\frac{L}{V_{out}} = \frac{(V_{in} - V_{out})}{V_{in} f r_R I_{out}}. \quad (14)$$

Performing this substitution, summing (13) and (12), and dividing by output capacitance, we can obtain an expression for the voltage excursion

$$V_{q1+q2} = \frac{I_{out}}{2Cf}\left(\frac{r_R}{4}\left(\frac{V_{out}}{V_{in}}\right) + \frac{V_{in} - V_{out}}{V_{in} r_R}\left(\frac{\Delta I}{I_{out}} - \frac{r_R}{2}\right)^2\right). \quad (15)$$

To this we must add the capacitor voltage at the time we started integrating charge, which, at a ripple-current zero crossing, is the peak ripple voltage, equal to half the peak-to-peak steady-state voltage ripple,

$$V_{r-peak} = \frac{1}{4}\left(\frac{1}{2Cf}\right)\left(\frac{r_R I_{out}}{2}\right). \quad (16)$$

Combining this with (15), we obtain

$$\Delta V = \frac{I_{out}}{2Cf}\left(\frac{r_R}{4}\left(\frac{V_{out}}{V_{in}} - \frac{1}{2}\right) + \frac{V_{in} - V_{out}}{V_{in} r_R}\left(\frac{\Delta I}{I_{out}} - \frac{r_R}{2}\right)^2\right). \quad (17)$$

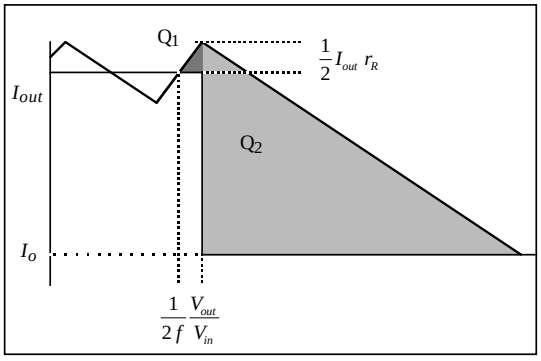

Fig. 8. Decreasing load step diagram showing charge areas used to calculate the voltage deviation resulting from to the load step.

For $\Delta I = I_{out}$, the typical worst-case load step, this can also be written as

$$\Delta V = \frac{I_{out}}{2Cf}\left(\frac{1}{8} r_R + \left(1 - \frac{V_{out}}{V_{in}}\right)\left(1 + \frac{1}{r_R}\right)\right). \quad (18)$$

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